19-0616; Rev 0; 7/06

EVALUATION KIT AVAILABLE

USB 2.0 High-Speed, Fault-Tolerant 3:1, 4:1 Multiplexers

General Description

The MAX4899E/MAX4899AE analog multiplexers combine the low on-capacitance (C_{ON}) and low on-resistance (R_{ON}) necessary for high-performance switching applications. These devices are designed for USB 2.0 high-speed applications at 480Mbps. The MAX4899E/MAX4899AE also handle all the requirements for USB low- and full-speed signaling.

The MAX4899E is a dual 3:1 multiplexer whereas the MAX4899AE is a dual 4:1 multiplexer. The MAX4899E/MAX4899AE feature two digital inputs, C_0 and C_1, to control the analog signal path. Typical applications include switching a USB connector between USB and other operations such as serial communications, audio, and video.

An enable input ($\overline{EN}$) is provided to disable all channels and place the device into a high-impedance (off) state, as well as reducing power consumption.

The MAX4899E/MAX4899AE operate from a 2.7V to 3.6V power-supply voltage and are protected against +5.5V shorts to COM_A- and COM_A+. In addition, COM_A+ and COM_A- are normally connected to outside circuitry and feature ±15kV ESD protection. The MAX4899E/MAX4899AE are available in a 3mm x 3mm, 16-pin TQFN package and operate over the -40°C to +85°C temperature range.

Applications

Cell Phones

Digital Still Cameras

PDAs

Digital Video Cameras

MPEG-4 Players

Portable GPS

Combination Products

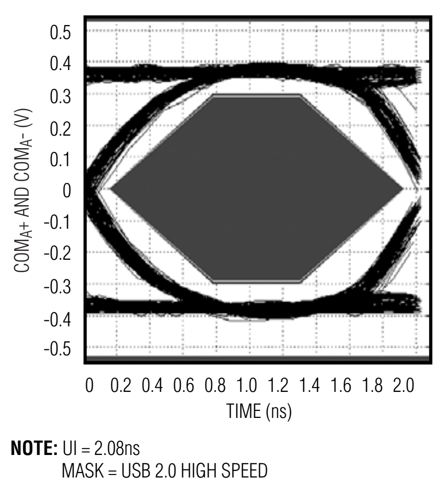
KVM

Pin Configurations appear at end of data sheet.

Features

- ♦ **Single 2.7V to 3.6V Power-Supply Voltage**
- ♦ **Low 4Ω (typ) On-Resistance (R_{ON})**
- ♦ **-3dB Bandwidth: 425MHz**
- ♦ **Fault Tolerant to Meet Full USB 2.0 Specification**
- ♦ **COM_ Protected to ±15kV ESD Protection per Human Body Model (MIL-STD-883; Method 3015)**
- ♦ **Low Operating Current (200µA), Ultra-Low Quiescent Current (3.0µA max) in Standby Mode**
- ♦ **Low Threshold Eliminates the Need for Translators in 1.8V Low Voltage Systems**
- ♦ **Tiny 16-Pin, 3mm x 3mm, Lead-Free TQFN Package**

Eye Diagram



Ordering Information/Selector Guide

PART	PIN-PACKAGE	MUX CONFIGURATION	TOP MARK	PKG CODE
MAX4899EETE+	16 TQFN-EP*	DUAL 3:1	AEY	T1633-4
MAX4899AEETE+	16 TQFN-EP*	DUAL 4:1	AEZ	T1633-4

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

+Denotes lead-free package.

**EP = Exposed paddle.*

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND.)
V+ ....-0.3V to +4V
$\overline{QP}$, $\overline{EN}$, C_0, C_1, (Note 1) ....-0.3V to +4V
COM_{A+}, $COM_{A_}$, USB0+, USB0-, USB1+, USB1-, USB2+,
USB2-, USB3+, USB3- ....-0.3V to +5.5V
Continuous Current ($COM_{A_}$ to USB_)..........................±120mA
Peak Current ($COM_{A_}$ to USB_)
(pulsed at 1ms, 10% duty cycle)................................±240mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: Signals exceeding GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +3.6V, T_A = -40°C to +85°C, $\overline{QP}$ = low, $\overline{EN}$ = low, unless otherwise noted. Typical values are at V+ = +3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH ($COM_{A_}$, USB__)							
On-Resistance	R_{ON}	V+ = 2.7V, $I_{COMA_}$ = -10mA, $V_{COMA_}$ = 0V, 1.5V, $\overline{QP}$ = low	T_A = +25°C		4	5	Ω
			T_A = -40°C to +85°C			6	
		V+ = 2.7V, $I_{COMA_}$ = -10mA, $V_{COM_}$ = 0V, 1.5V, 2.7V, $\overline{QP}$ = low	T_A = +25°C		4	7	
			T_A = -40°C to +85°C			8	
		V+ = 2.7V, $I_{COMA_}$ = -10mA, $V_{COMA_}$ = 0V, 1.5V, $\overline{QP}$ = high	T_A = +25°C		8	17	
			T_A = -40°C to +85°C			18	
		V+ = 3.0V, $I_{COMA_}$ = -10mA, $V_{COMA_}$ = 0V, 1.5V, $\overline{QP}$ = high	T_A = +25°C		4	12	
			T_A = -40°C to +85°C			13	
On-Resistance Match Between Channels	ΔR_{ON}	V+ = 2.7V, $I_{COMA_}$ = -10mA, $V_{COMA_}$ = 0V, 1.5V, 2.7V	T_A = +25°C		0.5	0.8	Ω
			T_A = -40°C to +85°C			1.0	
On-Resistance Flatness	$R_{FLAT (ON)}$	V+ = 2.7V, $I_{COMA_}$ = -10mA, $V_{COMA_}$ = 0V, 1.5V, 2.7V			0.5	1.1	Ω
Off-Leakage Current	$I_{L(OFF)}$	V+ = 3.6V, $V_{COMA_}$ = $V_{USB__}$ = 0.3V, 3.3V		-1		+1	µA
On-Leakage Current	$I_{L(ON)}$	V+ = 3.6V, $V_{COMA_}$ = $V_{USB__}$ = 0.3V, 3.3V		-1		+1	µA
Quiescent Supply Current	I+	V+ = 3.6V, C_0 = C_1 = 0 or V+	$\overline{QP}$ = low		250	600	µA
			$\overline{QP}$ = high			3	
Fault-Protection Trip Threshold	V_{FP}	V+ = 3.3V		3.6	3.9	4.2	V
ESD PROTECTION							
COM_A+, COM_A-		Human Body Model			±15		kV

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, T_A = -40°C to +85°C, $\overline{QP}$ = low, $\overline{EN}$ = low, unless otherwise noted. Typical values are at V+ = +3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCH AC PERFORMANCE (Note 3)						
On-Loss	ON_{LOSS}	f = 10MHz, 0 < V_{IN} < 1V, Figure 1		0.5		dB
Crosstalk	V_{CT1}, V_{DCT1}	f = 50MHz, Figure 1		-50		dB
Off-Isolation	V_{ISO}	f = 50MHz, Figure 1		-45		dB
Charge-Pump Noise	V_{QP}	$COM_{A_}$, USB_, R_L = R_S = 50Ω (Note 4)		100		µV
Bandwidth -3dB	BW	R_S = R_L = unbalanced 50Ω		425		MHz
Off-Capacitance	C_{OFF}	f = 1MHz, $COM_{A_}$, USB_, Figure 2		10.5		pF
On-Capacitance	C_{ON}	f = 1MHz, $COM_{A_}$, USB_, Figure 2		15		pF
Propagation Delay	t_{PD}	R_L = R_S = 50Ω, Figure 3		200		ps
Output Skew Same Switch	t_{SK}	Skew between opposite transitions in same switch, Figure 3		100		ps
Fault-Protection Response Time	t_{FP}	$V_{COMA_}$ = 0V to 5V to $V_{USB__}$ = 2.5V, R_L = 50Ω, C_L = 10pF, Figure 4		1		µs
Fault-Protection Recovery Time	t_{FPR}	$V_{COMA_}$ = 5V to 3V to $V_{USB__}$ = 1.5V, R_L = 50Ω, C_L = 10pF, Figure 4		1		µs
Charge Injection	Q	V_{GEN} = 0, C_L = 1000pF, Figure 5		25		pC
Enable Turn-On Time	t_{ON}	V_{USB0+} = V+, R_L = 50Ω, C_L = 10pF, Figure 6		2.8		µs
Enable Turn-Off Time	t_{OFF}	V_{USB0+} = V+, R_L = 50Ω, C_L = 10pF, Figure 6		3		ns
Address Transition Time	t_{TRANS}	V_{USB0+} = V+, R_L = 50Ω, C_L = 10pF, Figure 7		1.2		µs
Total Harmonic Distortion Plus Noise	THD+N	f = 20Hz to 20kHz, $V_{COMA_}$ = $1V_{P-P}$, R_L = 600Ω		0.02		%
SWITCH LOGIC ($\overline{QP}$, $\overline{EN}$, C_0, C_1)						
Logic-Input Voltage Low	V_{IL}				0.4	V
Logic-Input Voltage High	V_{IH}		1.4			V
Input Logic Hysteresis	V_{HYST}			100		mV
Input Leakage Current	I_{LEAK}	V+ = 3.6V, C_0 = 0 or V+, C_1 = 0 or V+	-1		1	µA

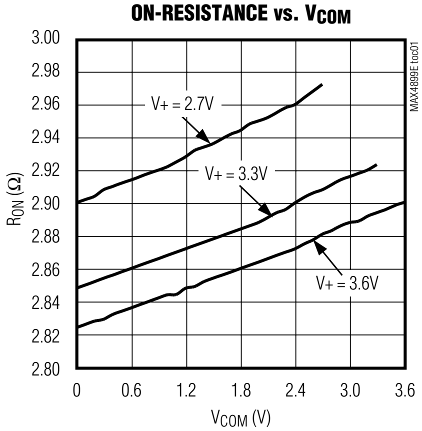
Note 2: Limits at -40°C are guaranteed by design.
Note 3: Guaranteed by design.
Note 4: Charge-pump noise is specified as a peak-to-peak value.

USB 2.0 High-Speed, Fault-Tolerant 3:1, 4:1 Multiplexers

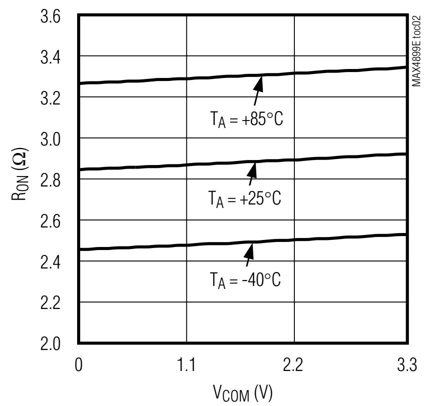
Typical Operating Characteristics

(V+ = 3.3V, $\overline{QP}$ = $\overline{EN}$ = low, T_A = +25°C, unless otherwise noted.)

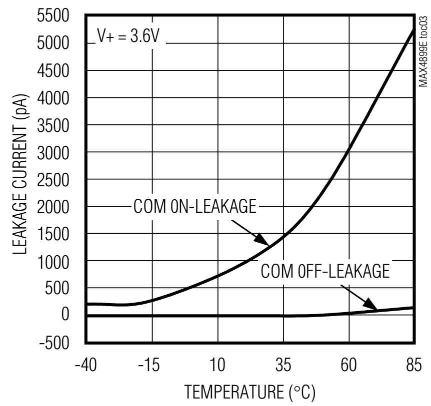
ON-RESISTANCE vs. V_{COM}



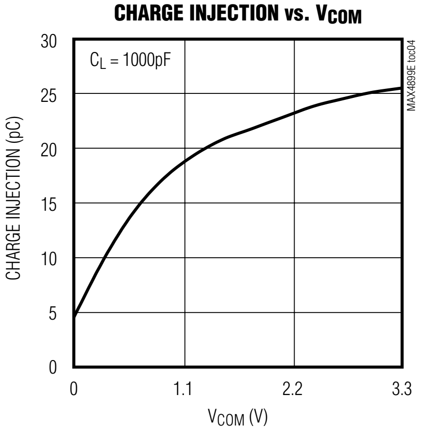
ON-RESISTANCE vs. V_{COM}



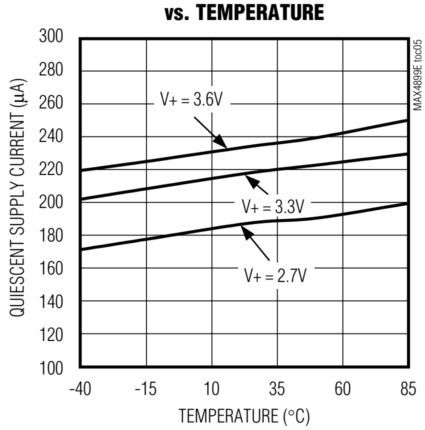
LEAKAGE CURRENT vs. TEMPERATURE



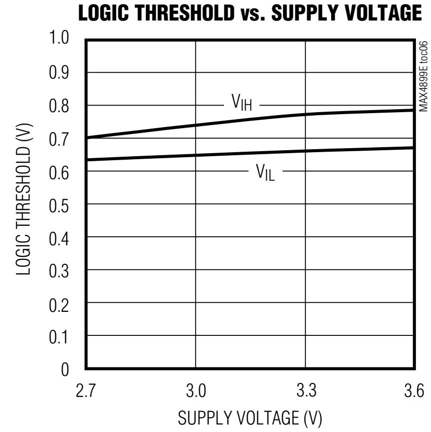
CHARGE INJECTION vs. V_{COM}



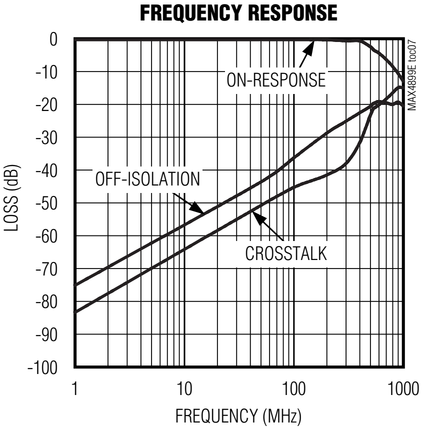
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



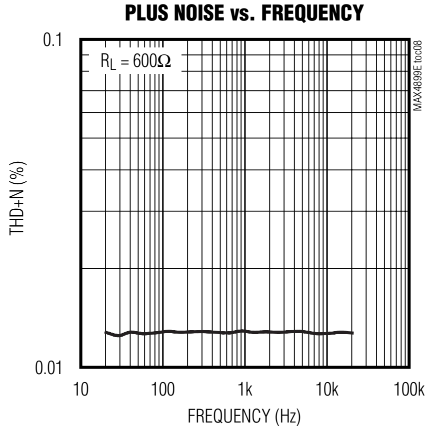
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



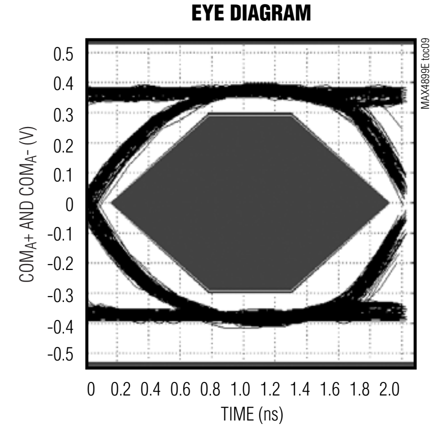
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



EYE DIAGRAM



Pin Description

PIN		NAME	FUNCTION
MAX4899E	MAX4899AE		
1	1	GND	Ground
2	2	COM_A+	Analog Switch Common D+ Terminal
3	3	COM_A-	Analog Switch Common D- Terminal
4	4	V+	Positive Supply-Voltage Input. Connect V+ to a 2.7V to 3.6V supply voltage. Bypass V+ to GND with a 0.1µF capacitor placed as close as possible to the device.
5	5	C_1	Digital Control Input 1. C_1 and C_0 control the analog signal path as shown in the *Functional Diagrams section*.
6	6	C_0	Digital Control Input 0. C_1 and C_0 control the analog signal path as shown in the *Functional Diagrams section*.
7, 8	—	N.C.	No Connection. Not internally connected.
—	7	USB3-	Analog Switch 3 D- Terminal
—	8	USB3+	Analog Switch 3 D+ Terminal
9	9	USB2-	Analog Switch 2 D- Terminal
10	10	USB2+	Analog Switch 2 D+ Terminal
11	11	USB1+	Analog Switch 1 D+ Terminal
12	12	USB1-	Analog Switch 1 D- Terminal
13	13	USB0+	Analog Switch 0 D+ Terminal
14	14	USB0-	Analog Switch 0 D- Terminal
15	15	$\overline{EN}$	Active-Low Enable Input. For normal operation, drive $\overline{EN}$ low. Drive $\overline{EN}$ high to place all channels in a high-impedance state. The internal charge pump is turned off when $\overline{EN}$ is a logic-high.
16	16	$\overline{QP}$	Active-Low Charge-Pump Enable Input. Drive $\overline{QP}$ low for normal operation. Drive $\overline{QP}$ high to disable the charge pump with the switches still active at a reduced analog signal range and higher R_{ON}.
—	—	EP	Exposed Paddle. Connect EP to GND.

Test Circuits/Timing Diagrams

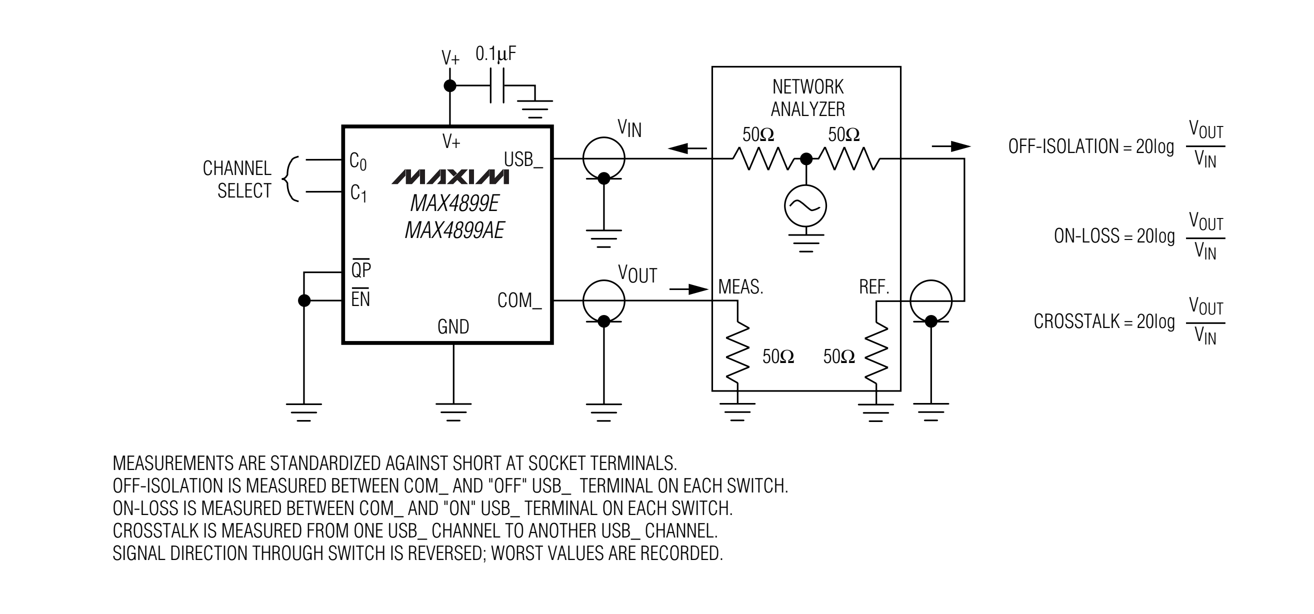


Figure 1. Off-Isolation, On-Loss, and Crosstalk

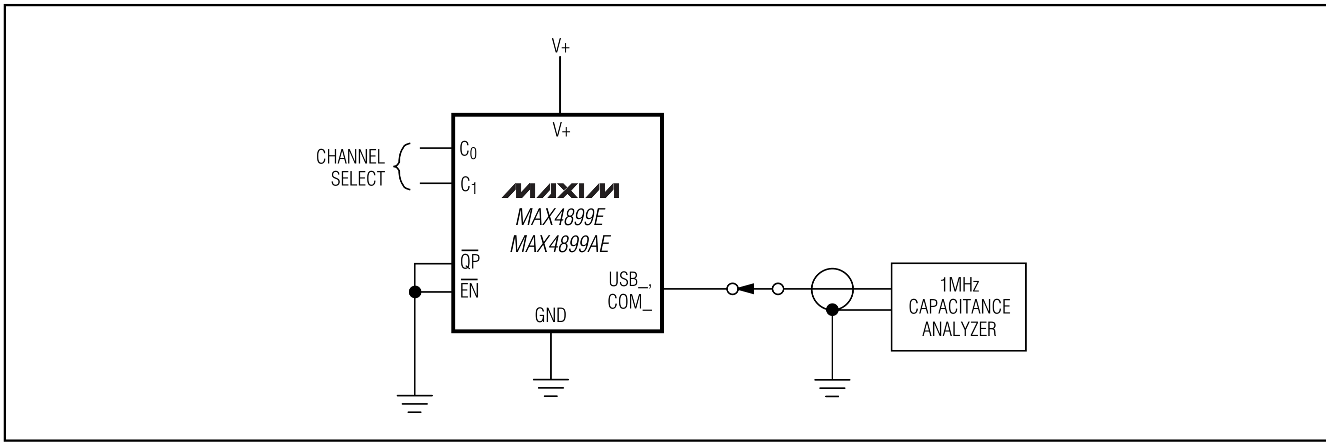


Figure 2. Channel Off-/On-Capacitance

Test Circuits/Timing Diagrams (continued)

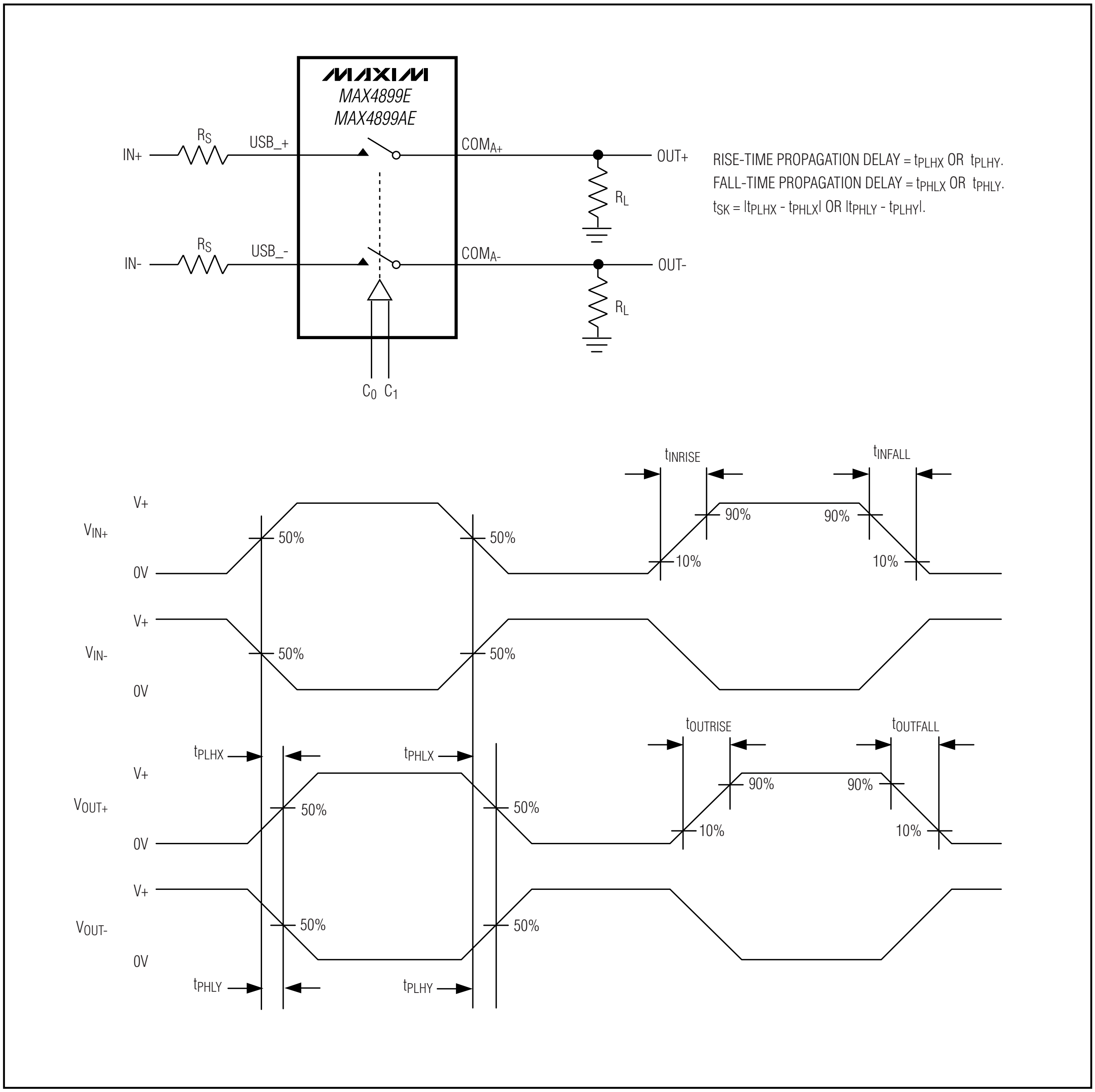


Figure 3. Propagation Delay and Output Skew

Test Circuits/Timing Diagrams (continued)

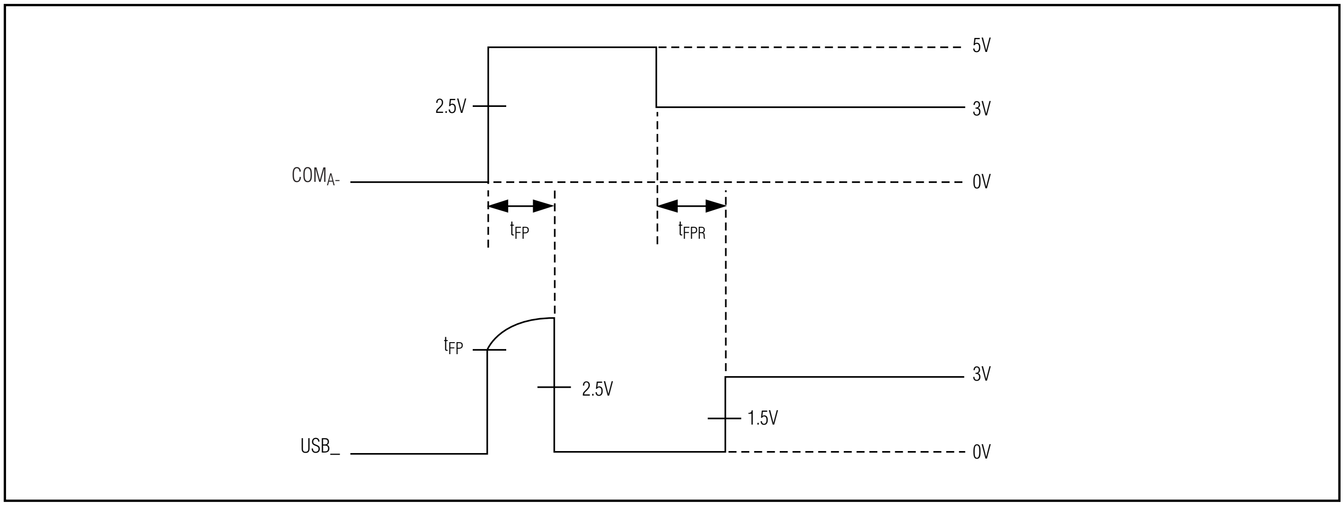


Figure 4. Fault-Protection Response/Recovery Time

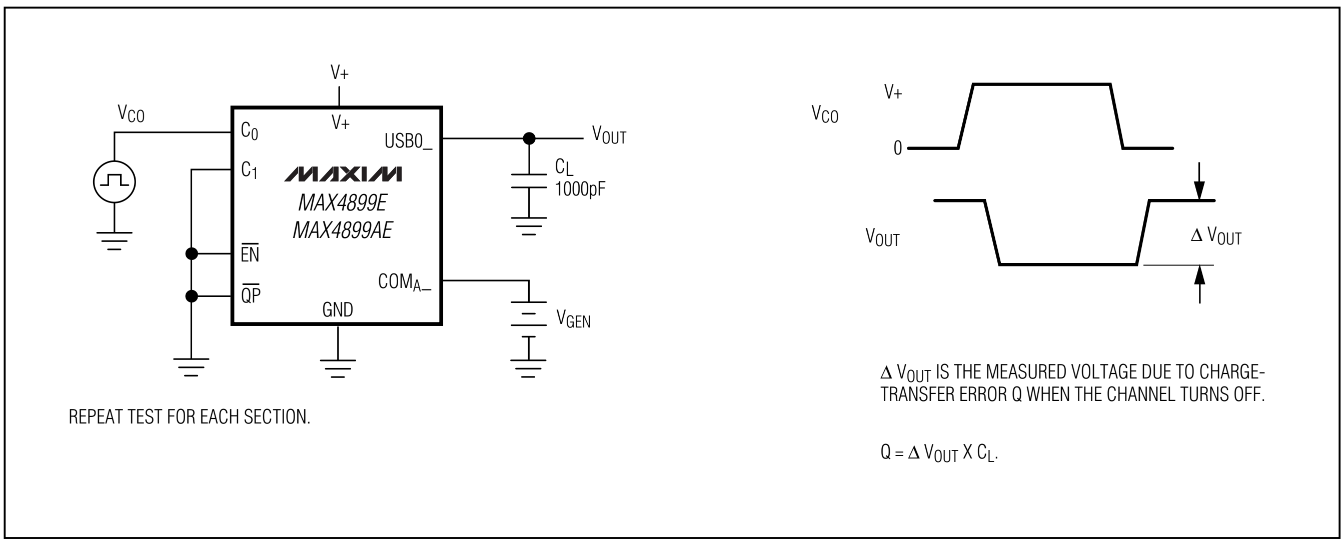


Figure 5. Charge Injection

Test Circuits/Timing Diagrams (continued)

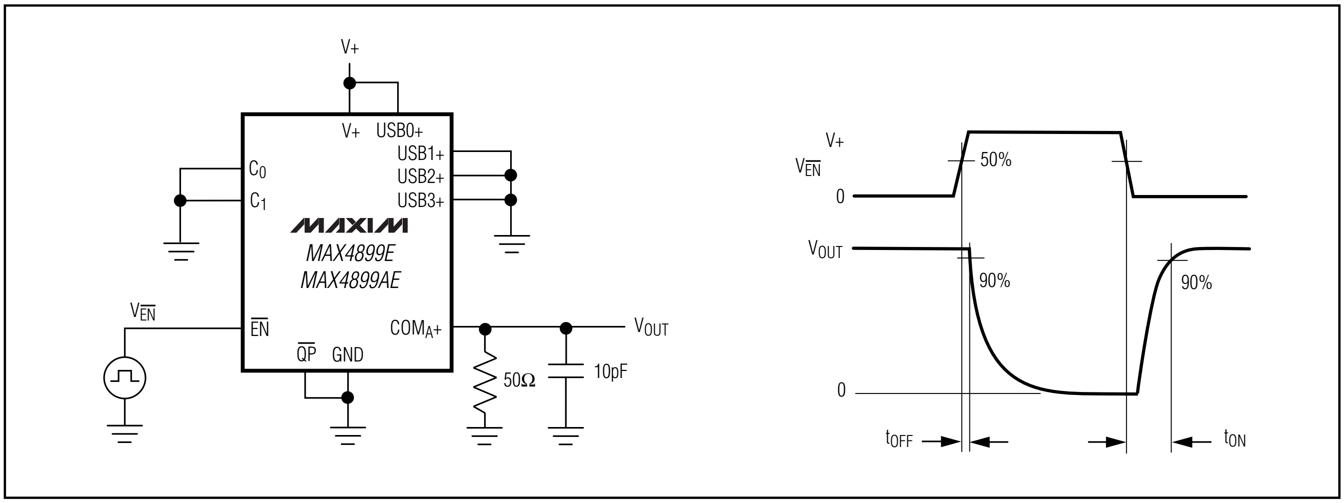


Figure 6. Enable Switching Times

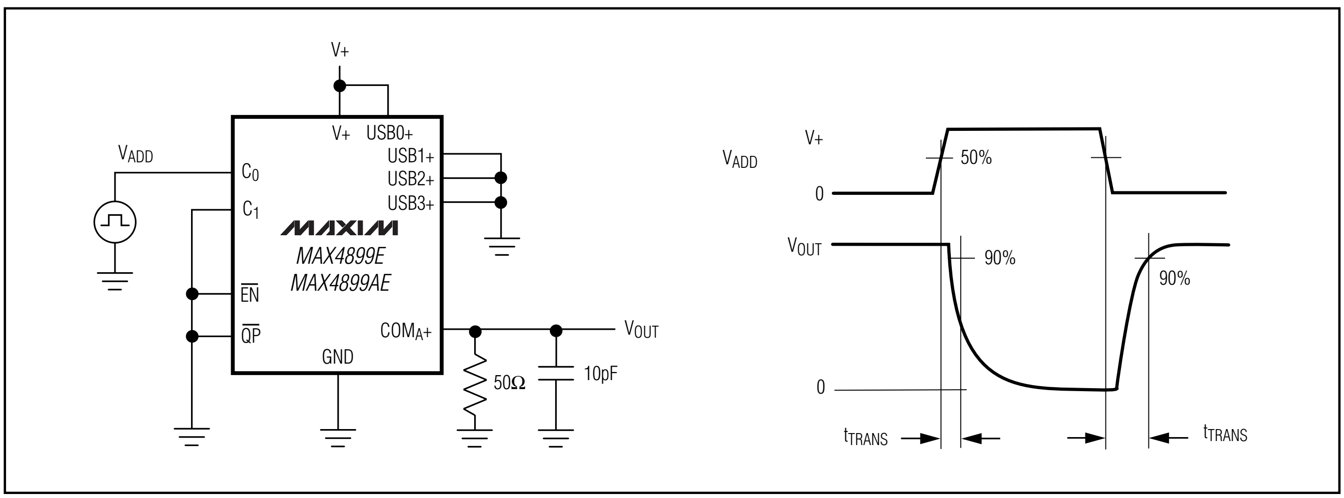


Figure 7. Address Transition Time

Detailed Description

The MAX4899E/MAX4899AE analog multiplexers combine the low on-capacitance (C_{ON}) and low on-resistance (R_{ON}) necessary for high-performance switching applications. These devices are designed for USB 2.0 high-speed applications at 480Mbps. The MAX4899E/MAX4899AE also handle all the requirements for USB low- and full-speed signaling. In the case of USB low/full speed, these devices can function normally even if the supply voltage is 2.7V, even though the USB signal may be higher than the supply voltage.

The MAX4899E is a dual 3:1 multiplexer, whereas the MAX4899AE is a dual 4:1 multiplexer. The MAX4899E/MAX4899AE feature two digital inputs, C_0 and C_1, to control the analog signal path. Typical applications include switching a USB connector between USB and other operations such as serial communications, audio, and video.

An enable input ($\overline{EN}$) is provided to disable all channels and place the device into a high-impedance (off) state, as well as shutting off the charge pump for minimum power consumption. The MAX4899E/MAX4899AE feature an additional charge-pump enable input ($\overline{QP}$) to disable the charge pump. The switches remain active at a lower analog signal range and higher R_{ON}.

The MAX4899E/MAX4899AE operate from a 2.7V to 3.6V power-supply voltage and are current-limit protected against +5.5V shorts to COM_A- and COM_A+.

Digital Control Inputs (C_0, C_1)

The MAX4899E/MAX4899AE provide two digital control inputs (C_0, C_1) to select the analog signal path between the COM_A_ and USB__ channels. The truth tables for the MAX4899E/MAX4899AE are shown in the *Functional Diagrams.* Since the MAX4899E only has three USB__ channels, the code C_1:C_0 = 1:1 can be used to place all channels into a high-impedance state. This is particularly useful for eliminating the extra control line to the $\overline{EN}$ input that is normally used for disabling all channels. Driving C_0 and C_1 rail-to-rail minimizes power consumption.

Enable Input ($\overline{EN}$)

The MAX4899E/MAX4899AE feature an enable input ($\overline{EN}$) that when driven high places all channels into a high-impedance state, as an all-off feature. The internal charge pump is also disabled when $\overline{EN}$ is high, thus minimizing the quiescent supply current. For normal operation, drive $\overline{EN}$ low.

Charge-Pump Enable Input ($\overline{QP}$)

The charge-pump input ($\overline{QP}$) disables and enables the internal charge pump. Drive $\overline{QP}$ high to disable the charge pump and reduce the quiescent supply current. With the charge pump disabled, the MAX4899E/MAX4899AE still function normally; however, the analog signal range is reduced and the switch on-resistance (R_{ON}) is increased. The analog signal range with the charge pump disabled is 0V to 1.5V. For normal operation, drive $\overline{QP}$ low.

Analog Signal Levels

Signals applied to COM_A+ are routed to the USB_+ terminals, and signals applied to COM_A- are routed to the USB_- terminals. These multiplexers are bidirectional, allowing COM_A_ and USB_ to be configured as either inputs or outputs. The D+ and D- notation in the *Pin Description* table is arbitrary and can be interchanged. For example, USB D+ signals can be applied to COM_A- and are routed to the USB_- terminals. Additionally, these multiplexers can be used for non-USB signals. COM_A+ and COM_A- are normally connected to outside circuitry and are ±15kV ESD protected.

The MAX4899E is a dual 3:1 multiplexer, allowing COM_A+ to be routed to one of three USB_+ channels, and COM_A- to be routed to one of three USB_- channels. The MAX4899AE is a dual 4:1 multiplexer, allowing COM_A+ to be routed to one of four USB_+ channels, and COM_A- to be routed to one of four USB_- channels.

Overvoltage Fault Protection

The MAX4899E/MAX4899AE feature +5.5V fault protection to COM_A+ and COM_A-. When a fault occurs between 4.5V to 5.5V, the switch automatically goes into a current-limiting mode that limits current to less than 2mA. Fault protection prevents these switches and downstream devices from being damaged due to shorts to the USB bus voltage rail.

Applications Information

USB Switching

The MAX4899E/MAX4899AE analog multiplexers are fully compliant with the USB 2.0 specification. The low on-resistance and low on-capacitance of these multiplexers make them ideal for high-performance switching applications. The MAX4899E/MAX4899AE are ideal for routing USB data lines and for applications that require switching between different data types (see Figure 8).

Board Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled impedance PC board traces as short as possible. Ensure that bypass capacitors are placed as close to the device as possible and use large ground planes where possible.

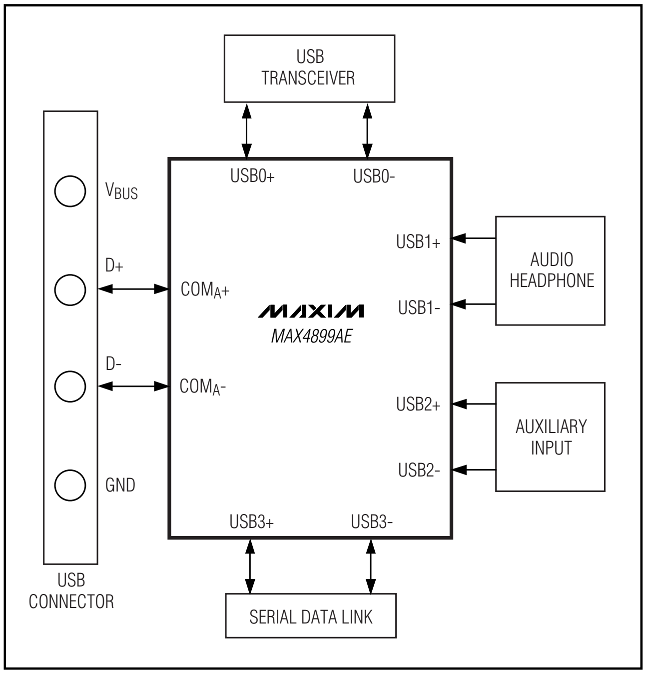


Figure 8. MAX4899AE Multiplexing Four Data Types

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The COM_A+ and COM_A- lines have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, tri-state output mode, and powered down. After an ESD event, Maxim's E-versions keep working without latch-up, whereas competing products can latch and must be powered down to remove latch-up.

Human Body Model

The MAX4899E/MAX4899AE COM_A+ and COM_A- pins are characterized for ±15kV ESD protection using the Human Body Model (MIL-STD-883, Method 3015). Figure 9a shows the Human Body Model and Figure 9b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

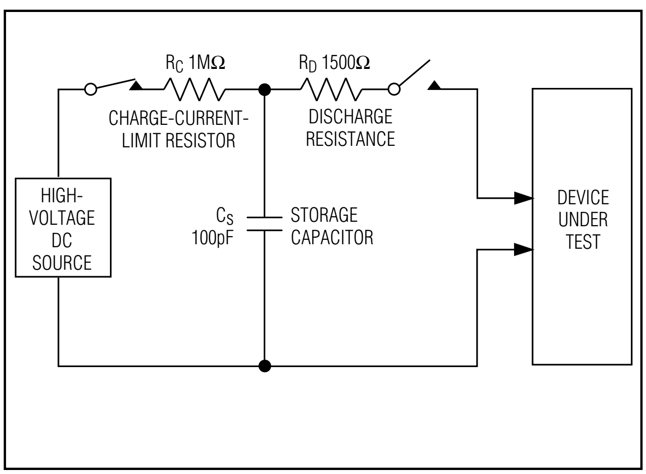


Figure 9a. Human Body ESD Test Model

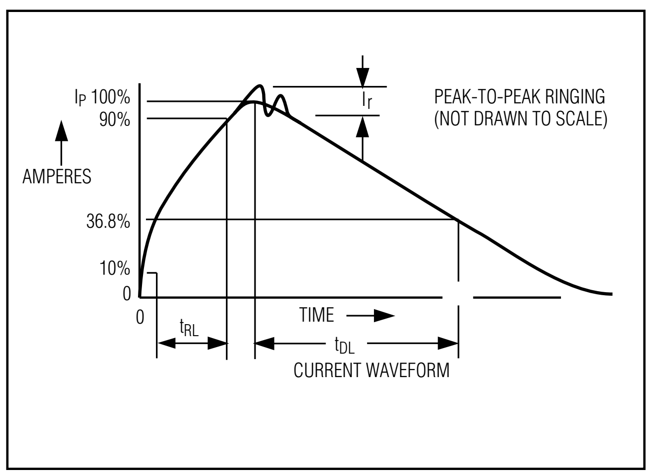


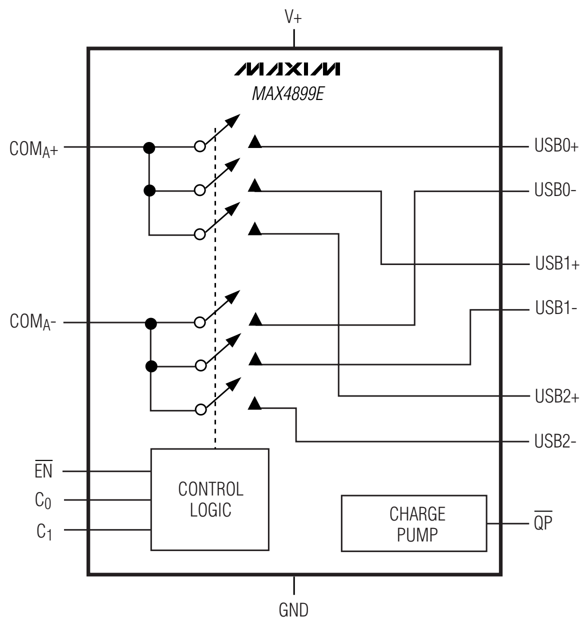
Figure 9b. Human Body Model Current Waveform

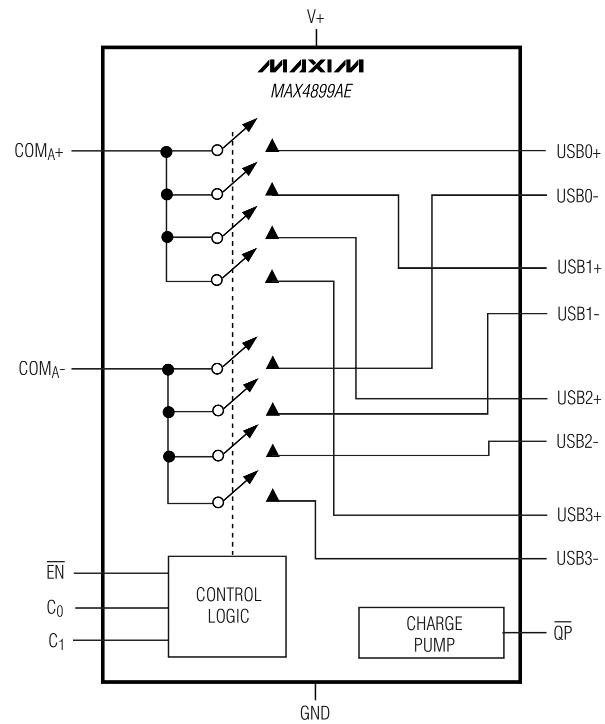
Chip Information

PROCESS: BiCMOS

USB 2.0 High-Speed, Fault-Tolerant 3:1, 4:1 Multiplexers

Functional Diagrams



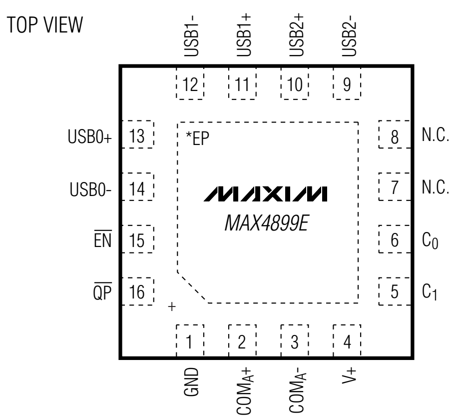


MAX4899E					
$\overline{QP}$	$\overline{EN}$	C_1	C_0	FUNCTION	COMMENT
0	0	0	0	COM_A+ → USB0+ COM_A- → USB0-	NORMAL OPERATION
0	0	0	1	COM_A+ → USB1+ COM_A- → USB1-	NORMAL OPERATION
0	0	1	0	COM_A+ → USB2+ COM_A- → USB2-	NORMAL OPERATION
0	0	1	1	HIGH-Z	ALL OFF
0	1	X	X	HIGH-Z	ALL OFF
1	1	X	X	HIGH-Z	ALL OFF
1	0	0	0	COM_A+ → USB0+ COM_A- → USB0-	LARGER R_{ON}
1	0	0	1	COM_A+ → USB1+ COM_A- → USB1-	LARGER R_{ON}
1	0	1	0	COM_A+ → USB2+ COM_A- → USB2-	LARGER R_{ON}
1	0	1	1	HIGH-Z	ALL OFF

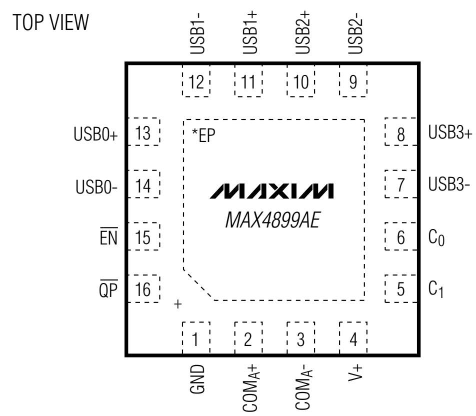
MAX4899AE					
$\overline{QP}$	$\overline{EN}$	C_1	C_0	FUNCTION	COMMENT
0	0	0	0	COM_A+ → USB0+ COM_A- → USB0-	NORMAL OPERATION
0	0	0	1	COM_A+ → USB1+ COM_A- → USB1-	NORMAL OPERATION
0	0	1	0	COM_A+ → USB2+ COM_A- → USB2-	NORMAL OPERATION
0	0	1	1	COM_A+ → USB3+ COM_A- → USB3-	NORMAL OPERATION
0	1	X	X	HIGH-Z	ALL OFF
1	1	X	X	HIGH-Z	ALL OFF
1	0	0	0	COM_A+ → USB0+ COM_A- → USB0-	LARGER R_{ON}
1	0	0	1	COM_A+ → USB1+ COM_A- → USB1-	LARGER R_{ON}
1	0	1	0	COM_A+ → USB2+ COM_A- → USB2-	LARGER R_{ON}
1	0	1	1	COM_A+ → USB3+ COM_A- → USB3-	LARGER R_{ON}

X = 1 or 0.

Pin Configurations



TQFN

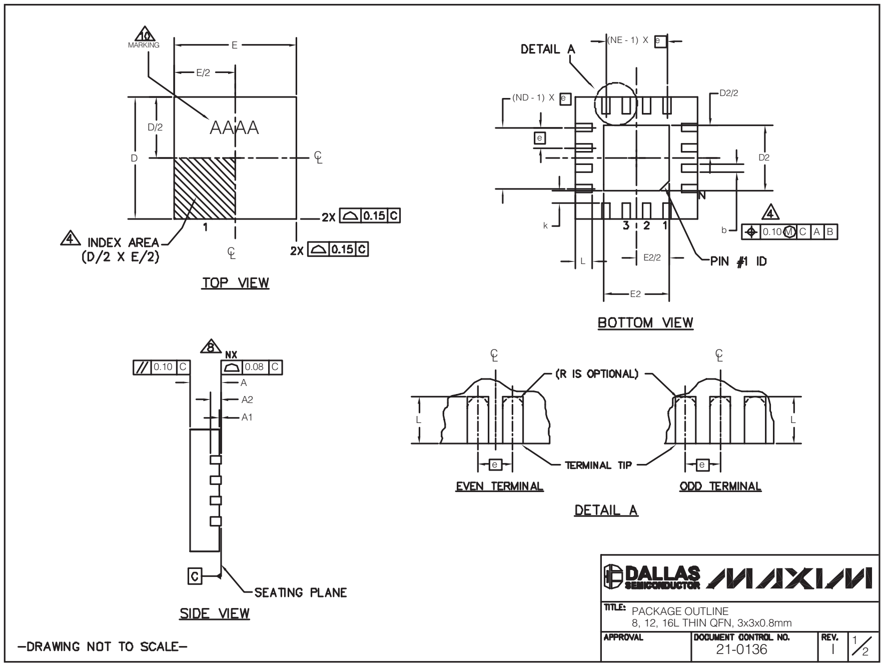


TQFN

*CONNECT EXPOSED PAD TO GND

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



12x16L QFN THIN.EPS

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS .
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0136 | REV. I | 2/2

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